Ramdeobaba University (RBU)

RBU

RAMDEOBABA UNIVERSITY, NAGPUR

Formerly Shri Ramdeobaba College of Engineering & Management (RCOEM) Est. 1984

School of Electrical and Electronics Engineering

Scheme of Teaching and Examination of Master of Technology (VLSI Design)

About the programme

The M.Tech in VLSI (Very Large Scale Integration) Design program provides an advanced education in the design and implementation of integrated circuits and systems. This program focuses on equipping students with specialized knowledge and skills required to develop cutting-edge electronic devices and systems, emphasizing miniaturization, high performance, and low power consumption.

Students delve into advanced topics such as digital system design, analog and mixed-signal circuit design, ASIC/FPGA design methodologies, and design verification techniques. They gain hands-on experience through industry-standard EDA (Electronic Design Automation) tools and simulation software, preparing them for the challenges of the semiconductor industry

Upon completion of the program, graduates are poised for career opportunities in semiconductor companies, design service firms, research and development organizations, and academia. They play a crucial role in driving innovation in electronic systems, contributing to advancements in fields such as artificial intelligence, telecommunications, and Internet of Things (IoT).

USP: Specialized focus on VLSI design, addressing the demand for skilled professionals in semiconductor industry.

Key Features:

- Advanced curriculum covering digital system design, ASIC/FPGA methodologies, and design verification techniques.
- Hands-on experience with industry-standard EDA tools and simulation software.
- Access to cutting-edge laboratories and collaboration opportunities with industry partners.
- Guidance from experienced faculty members with expertise in VLSI design and research.

Opportunities:

- Career paths in semiconductor companies, design service firms, and research organizations.
- Opportunities for roles such as VLSI design engineer, verification engineer, or CAD engineer.
- Potential for leadership positions in project management or research and development.
- Ability to contribute to technological advancements in areas like AI, IoT, and wireless communication through innovative chip design.

(CHOICE BASED CREDIT SYSTEM)

Programme Objectives:

1. To develop graduates with an ability to design and analyze VLSI Systems.
2. To prepare graduates to adapt to the evolving technical challenges by acquiring necessary skills to excel in their career.
3. To encourage life-long learning with commitment to ethical practices.

Programme Outcomes:

PO1: An ability to apply knowledge of VLSI Design to solve engineering problems.

PO2: An ability to acquire skills to interpret, analyze and evaluate problems of VLSI Systems

PO3: An ability to independently carry out research / investigation and development of work to solve socio - economic problems.

PO4: An ability to write and present a substantial technical report /document.

SESSION 2024-2025

I SEMESTER

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51 TH0101	CMOS Digital Circuit Design	4	0	4	50	50	100	3 Hrs.	PCC
2	24EE51 PR0101	CMOS Digital Circuit Design Lab	0	2	1	25	25	50	-	PCC
3	24EE51 TH0102	Digital SystemDesign	4	0	4	50	50	100	3 Hrs.	PCC
4	24EE51 PR0102	Digital SystemDesign Lab	0	2	1	25	25	50	-	PCC
5	24EE51 TH0103	Semiconductor Devices	4	0	4	50	50	100	3 Hrs.	PCC
6	24EE51 TH0104	Embedded System and RTOS	4	0	4	50	50	100	3 Hrs.	PCC
7	24EE51 PR0104	Embedded System and RTOS Lab	0	2	1	25	25	50	-	PCC
8	24EE51 TH0105	Programme Elective-1	4	0	4	50	50	100	3 Hrs.	PEC
9	24EE51 PR0106	Lab Practice - I	0	4	2	25	25	50	-	PCC
10	-	Technical Communication	3	0	3	50	50	100	3 Hrs.	SEC
		Total	**22**	**12**	**28**					

Course Code	Programme Elective – I
24EE51TH0105-01	MEMS Design and Fabrication
24EE51TH0105-02	Advanced Computer Architecture
24EE51TH0105-03	Advanced Digital Signal Processing
24EE51TH0105-04	Hardware Assisted Security
24EE51TH0105-05	Machine Learning

DEPARTMENT OF ELECTRONICS ENGINEERING

M. TECH. (VLSI DESIGN)

II SEMESTER

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51TH0201	Analog IC Design	4	0	4	50	50	100	3 Hrs.	PCC
2	24EE51PR0201	Analog IC Design Lab	0	2	1	25	25	50	-	PCC
3	24EE51TH0202	System Verilog for Verification	4	0	4	50	50	100	3 Hrs.	PCC
4	24EE51PR0202	System Verilog for Verification Lab	0	2	1	25	25	50	-	PCC
5	24EE51TH0203	Programme Elective-II	4	0	4	50	50	100	3 Hrs.	PEC
6	24EE51TH0204	Programme Elective-III	4	0	4	50	50	100	3 Hrs.	PEC
7	24EE51PR0205	Lab Practice - II	0	4	2	25	25	50	-	PCC
8	24EE51PR0206	Seminar	0	4	2	50		50	-	AEC
9	24EEOEC51TH0207	Open Elective-I	3	0	3	50	50	100	3 Hrs.	OE
		Total	**20**	**10**	**25**					

Course Code	Programme Elective – II/III
24EE51TH0203-01/ 24EE51TH0204-01	VLSI Signal Processing
24EE51TH0203-02/ 24EE51TH0204-02	RF Circuit Design
24EE51TH0203-03/ 24EE51TH0204-03	Memory Technologies
24EE51TH0203-04/ 24EE51TH0204-04	Flexible Electronics and Sensors
24EE51TH0203-05/ 24EE51TH0204-05	Embedded Machine Learning
24EE51TH0203-06/ 24EE51TH0204-06	VLSI Physical Design
24EE51TH0203-07/ 24EE51TH0204-07	Industry Elective

Exit option: Award of PG Diploma			
Exit Courses			
1	Universal Verification Methodologies	Any one Online/Offline Certification Course	8
2	Design for testability		

Course Code	Open Elective-I
24EEOEC51TH0207	Digital System Design with FPGA

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III SEMESTER

Sr. No	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51 TH0301	Research Methodology & IPR	2	0	2	50	50	100	3 Hrs.	MLC
2	24EE51 TH0302	Programme Elective-IV	4	0	4	50	50	100	3 Hrs.	PEC
3	24EE51 TH0303	Programme Elective-V	4	0	4	50	50	100	3 Hrs.	PEC
4	24EE51 PR0304	Project Phase I	0	4	2	50	50	100	----	PRJ
5	24EE51 TH0305	Participatory Learning	1	0	1	50	-	-	----	CCA
		Total	**11**	**4**	**13**					

OR

Sr. No	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51 TH0306	Research Methodology& IPR	2	0	2	50	50	100	3 Hrs.	MLC
	OR									
	24EE51 TH0307	Research Methodology (MOOC/Any online platform	-	-	2			100		
2	24EE51 PR0308	Industry Internship / Research Internship	-	-	9	100	100	200		INT
		Total			**11**					

Course Code	Programme Elective-IV / V
24EE51TH0302-01/24EE51TH0303-01	Design for testability
24EE51TH0302-02/24EE51TH0303-02	SoC Design
24EE51TH0302-03/24EE51TH0303-03	Nano materials and Nanotechnology
24EE51TH0302-04/24EE51TH0303-04	Low Power VLSI Design
24EE51TH0302-05/24EE51TH0303-05	Mixed Signal Processing
24EE51TH0302-06/24EE51TH0303-06	MOOC -I
24EE51TH0302-07/24EE51TH0303-07	MOOC -II

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IV SEMESTER

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51PR0401	Project Phase-II	0	28	14	150	150	300	----	PRJ
		Total	**0**	**28**	**14**					

OR

Sr. No.	Code	Course	L	P	Credits	Maximum Marks			Exam Duration	Category
						Continuous Assessment	End Sem	Total		
1	24EE51PR0402	Industry Internship / Research Internship	0	28	14	150	150	300	----	PC
		Total	**0**	**28**	**14**					

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0101 **Course: CMOS Digital Circuit**

Design L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to:

I. Apply the circuit models to investigate CMOS circuits.

II. Design moderately sized CMOS circuits/ sub-systems and compute timing, power and parasitic for various CMOS Logic structures.

III. Evaluate various micron, deep sub-micron and nanometer-scale technologies.

Syllabus:

Introduction to MOS Transistors, Switches, CMOS Logic, Scaling and transistors structures for VLSI; Silicon-on-insulator transistors.

Static Load MOS Inverters, CMOS Inverter, the Tri State Inverter.

Circuit Characterization and Performance Estimation: Introduction, Resistance EstimationCapacitance Estimation, Switching Characteristics, Transistor Sizing, Power Dissipation, Sizing Routing Conductors, Charge Sharing.

CMOS Circuit And Logic Design: CMOS Logic Gate Design, CMOS Logic Structures, Clocking Strategies, I/O Structures, Driving Large capacitive loads.

CMOS SubSystem Design: Data Path Operations-Addition/Subtraction, Parity Generators, Comparators, Binary Counters, ALUs, Multiplication, Shifters, Memory Elements, Control-FSM, Control Logic Implementation.

Memory elements: Read, write memory, RAM, Register files, FIFO, LIFO, SIPO, Serial access Memory, CAM, ROM.

Text books:

1. Principles of CMOS VLSI Design: N. Weste and K. Eshranghian, Addison Wesley, 2nd Edition
2. Digital Integrated Circuits: A Design Perspective: J. Rabaey, PHI, 2nd Edition
3. Basic VLSI Systems and Circuits: DouglesPucknell and K. Eshraghian PHI, 3rd Edition

Reference books:

1. VLSI Analog and Digital Circuit Design Techniques: Randel & Geiger TMH
2. Introduction to VLSI System: Carver Mead, Lynn Conway, Addison-Wesley, 1st Edition
3. CMOS Digital Integrated Circuits Analysis & Design: S M Kang, Yusuf Lablebici, TMH, 3rd Edition (2003)

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0101 **Course: CMOS Digital Circuit Design Lab**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practical / Case Studies/ Mini projects based on syllabus of 24EE51PR0101

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0102 Course: Digital System Design

L : 4 Hrs., P : 0 Hrs., Per week Credits : 4

Course Outcome

Upon the completion of this course, students will demonstrate the ability to:

- Model the Digital Designs using HDL
- Test the Digital Designs using HDL
- Analyze the timing issues in Digital Designs
- Optimize the Digital Designs for area, power and delay
- Implement the Digital Designs on FPGA platforms

Syllabus:

Hardware Description Languages

Introduction to HDL: Basic Language Elements, Syntax and Semantics HDL, Modeling Stylesfor building blocks, use of Procedures –functions / Task –function in designs, Attributes, Writing Test Benches, Handling Text files, Combinational & Sequential Design examples :Adders, Multipliers, ALU, Memories, FSM, FIFO

System Design Flow: Top-Down and Bottom-Up methodology, Word Length Determination, Data Path Control Path, Implementation of DSP algorithm

Synthesis- Analysis and Introduction to Optimization Techniques: Methodology, Logic Synthesis of HDL, Critical Path analysis, Speed, Area and Power optimizations at Architectural level, Timing and Signal Integrity: Timing Basics and Signal integrity, Dealing with Clock Skew and Jitter, Synchronizers

Programmable ASICs: Technology Overview, CLBs, Architecture, Realization of functions in FPGA

Text books:

1. A VHDL Primer, Third Edition: J. Bhasker, Prentice Hall, (1999).
2. Verilog HDL: A guide to Digital Design and Synthesis: Samir Palnitkar, Prentice Hall(1996)
3. Advanced Digital Design with the Verilog HDL: M.D. Ciletti, Prentice Hall, (2003).
4. Synthesis and Optimization of Digital Circuits, G. De Micheli, McGraw-Hill, (1994).

Reference books:

1. The Verilog Hardware Description Language, Fifth Edition: Donald E. Thomas, Philip R. Moorby, Kluwer Academy Publisher. (2002).
2. Digital Systems Design Using VHDL, Second Edition: Charles H. Roth. Jr., L Kurian John, Cengage Learning, (2008).
3. Logic Synthesis using Synopsys, Second edition, P. Kurup and T. Abbasi, Kluwer, (1996)
4. Logic synthesis and verification algorithms: Gary D. Hachtel, Fabio Somenzi, Springer (1996)
5. An Engineering Approach to Digital Design: W. Fletcher. Prentice Hall

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0102	**Course: Digital System Design Lab.**
L : 0 Hrs., P : 2 Hrs., Per week	**Credits : 1**

Practical / Case Studies/ Mini projects based on syllabus of 24EE51PR0102

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0103 **Course: Semiconductor Devices**

L :4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to

I. Estimate drift and diffusion carrier concentration in semiconductors, given the type and doping level of impurities.
II. Utilize the basic governing equations to analyze pn junctions &schottky junctions under various operating conditions.
III. Predict qualitative and quantitative operating conditions of MOS transistors & MOS Models and understand the concept of advanced MOSFET technology

Syllabus:

Basic Semiconductor Physics

Crystal lattice, energy band model, density of states, distribution statics – Maxwell-Boltzmann and Fermi-Dirac, doping, carrier transport mechanisms, drift, diffusion, thermionic emission, and tunneling; excess carriers, carrier lifetime, recombination mechanisms – SHR, Auger.

p-n junction and metal-semiconductor junction

p-n junctions- fabrication, basic operation – forward and reverse bias, DC model, charge control model, I-V characteristics, steady-state and transient conditions, capacitance model, reverse-bias breakdown, SPICE model; metal-semiconductor junctions –fabrication, Schottky barriers, rectifying ad ohmic contacts, I-V characteristics.

MOS Capacitors and MOSFETs

The MOS capacitor – fabrication, surface charge – accumulation, depletion, inversion, threshold voltage, C-V characteristics – low and high frequency; the MOSFET – fabrication, operation, gradual channel approximation, simple charge control model (SCCM), Pao-Sah and Schichman – Hodges models, I-V characteristics, second-order effects – Velocity saturation, short-channel effects, charge sharing model, hot-carrier effects, gate tunneling; subthreshold operation – drain induced barrier lowering (DIBL) effect, unified charge control model(UCCM), SPICE level 1, 2, and 3, and Berkeley short-channel IGFT model (BSIM).

Advanced MOSFET technology: SOI MOSFET, high-k MOS devices, FinFETs and Multi gate MOSFETs

Text Books:

1. Physics of Semiconductor Devices: S. M. Sze, Wiley Eastern, (1981).
2. Semiconductor physics and Devices, Donald Neamen, McGraw-Hill, 3rd edition
3. Solid State Electronic Devices ,B.G.Streetman and S.Banerjee ,Prentice Hall India

Reference Books:

1. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press.

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0104 **Course: Embedded System and RTOS**

L :4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Apply the knowledge of ARM architecture and organization for modern ARM Cortex-M devices.
- Utilize knowledge, techniques and skill to integrate hardware and software component using Cortex-M.
- Apply the concepts of Embedded OS.
- Design an embedded system for given constraint

Syllabus:

Introduction to Embedded Systems, Concepts, Embedded System Design Issues. RISC Principles.

The Cortex - M processor: Applications, Simplified view – block diagram, programming model – Registers, Operation modes, Exceptions and Interrupts, Reset Sequence , Instruction Set, Unified Assembler Language, Pipeline, Bus, Priority, Vector Tables, Interrupt Inputs and Pending behavior, Fault Exceptions, Supervisor and Pendable Service Call, Nested Vectored Interrupt Controller, SYSTICK Timer, Interrupt Sequences, Introduction to the Cortex microcontroller software interface standard (CMSIS), Interfacing of GPIOs, Timers, ADC, UART and other serial interfaces , PWM.

Concept and Fundamentals of RTOS: RTOS examples, Interrupts, Handling an Interrupt, Interrupt Service Routines, Context Switching, Process States, Communication Mechanism, Scheduling Algorithm, Priority Inversion, Priority Inheritance. Inter-task Communication: Shared Variables, Monitors, Messages, Events, Semaphores, Priority inversion problem, Deadlocks, Starvation.

Concepts, Structure of µCOS - II: - Kernel Structure: Tasks, Task States, TCB, Ready List, Task Scheduling, Interrupts, Clock Tick, Initialization, Starting the OS, Task Management, Time Management, Event Control Blocks, Synchronization in µCOS - II: - Semaphore Management, Mutual Exclusion Semaphores, Event Flag Management, Communication in µCOS - II: - Message Mailbox Management, Message Queue Management, Memory management, Porting of µCOS – II

Linux as an embedded OS, Tools and development, Applications and products, Building Linux Kernel

Text Books:

1. The Definitive Guide to the ARM Cortex-M0 : Joseph Yiu, Elsevier ,(1/E)2011
2. An embedded software primer: David E Simon, Pearson education Asia, 2001
3. Micro C/OS II The Real Time Kernel: Jean J. Labrosse, CMPBooks,(2/E) 2002
4. Embedded Linux Primer: christopher Hallinan, Pearson (1/E) 2007

Reference Books:

1. ARM System Developer's Guide Designing and Optimizing System Software: Andrew N. Sloss, Dominic Symes, Chris Wright, Morgan Kaufmann publications, (1/E) 2004.
2. ARM system on chip Architecture: Steve Furber, Person Education Addison Wesley, (2/E) 2000

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0104 **Course: Embedded System and RTOS Lab**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practical / Case Studies/ Mini projects based on syllabus of 24EE51PR0104

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : 24EE51PR0106 **Course : Lab Practice I**

L : 0 Hrs., P : 4 Hrs., Per week **Credits : 2**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

I. Apply fundamental principles to solve problems

II. Design and execute an experimental procedure, work independently, interpret experimental results

III. Draw a reasonable, accurate conclusion using suitable tools and technique

Practical / Case Studies / Mini projects

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : 24EE51TH0105-01 **Course : MEMS Design and Fabrication**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to

I. Apply the principles behind the operation of MEMS devices

II. Choose a micromachining technique for a specific MEMS fabrication process

III. Design and fabricate MEMS devices or a microsystem

IV. Understand recent advancements in the field of MEMS and devices.

Syllabus:

Micro-fabrication and Micromachining: Integrated Circuit Processes, Bulk Micromachining: Isotropic Etching and Anisotropic Etching, Wafer Bonding, High Aspect-Ratio Processes (LIGA)

Physical Micro-sensors: Classification of physical sensors, Integrated, Intelligent, or Smart sensors, Sensor Principles and Examples : Thermal sensors, Electrical Sensors, Mechanical Sensors, Chemical and Biosensors

Micro-actuators : Electromagnetic and Thermal micro-actuation, Mechanical design of micro-actuators, Micro-actuator examples, micro-valves, micro-pumps, micro-motors-Micro-actuator systems : Success Stories, Ink-Jet printer heads, Micro-mirror TV Projector

Surface Micromachining: One or two sacrificial layer processes, Surface micromachining requirements, Polysilicon surface micromachining, Other compatible materials, Silicon Dioxide, Silicon Nitride, Piezoelectric materials, Surface Micromachined Systems: Success Stories, Micromotors, Gear trains, Mechanisms

Application Areas: All-mechanical miniature devices, 3-D electromagnetic actuators and sensors, RF/Electronics devices, Optical/Photonic devices, Medical devices e.g. DNA-chip, micro-arrays.

MEMS for RF Applications: Need for RF MEMS components in communications, space and defense applications.

Text Books

1. Micro and Smart Systems, Ananthasuresh, G. K., Vinoy, K. J. Gopala Krishnan, S., Bhat, K. N., Aatre, V. K., Wiley-India, New Delhi, 2010. 1st Edition
2. RF MEMS and Their Applications: Vijay. Varadan, K. J. Vinoy, K. A. Jose, Wiley, 2002, 1st Edition.

Reference Books

1. Microsensors, MEMS and Smart Devices, Julian W. Gardner, Vinay K. Varadan, Osama O. Awadelkarim, Wiley, 2001, 1st Edition
2. VLSI Technology, Sze S. M., Mc Graw Hill, 2nd Edition

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0105-02 **Course: Advanced Computer Architecture**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to

- Define the principles of computer design and its performance enhancement measures.
- Describe the operations of performance such as pipelines, dynamic scheduling branch predictions, caches.
- Describe the modern architecture such as RISC, Scalar, VLIW, Multi core and multi CPU systems.
- Compare the performance of different computer architectures.
- Develop the applications for high performance computing systems.
- Appraise memory organizations and modern computer architectures.

Syllabus:

- Classes of computers, Trends in technology, power and costs, dependability, quantitative principles of computer design, Models of parallel computer, multiprocessors and multi-computers, multi-vector and SIMP computers, PRAM and VLSI model, conditions of parallelism, data and resource dependencies, grain size and latency, grain packing and scheduling, program flow mechanisms, system interconnect architectures.
- Principles of scalable performance, performance metrics and measures, speedup performance laws, advanced processor technology, superscalar and vector processors, cache memory organizations, shared memory organizations.
- Pipeline and superscalar techniques, linear pipeline processors, reservation and latency analysis, collision free scheduling, pipeline schedule optimization, instruction pipeline design, arithmetic pipeline design, superscalar and super-pipeline design.
- Multiprocessors and multi computers, multiprocessor system interconnects, cache coherence and synchronization mechanisms, message passing schemes.
- Multi-vector and SIMD computers vector processing principles, compound vector processing, SIMD computer organizations scalable multithreaded and dataflow architectures.
- Elementary theory about dependence analysis, techniques for extraction of parallelism.

Text Books :

1. Advanced Computer Architecture: Kai Hwang; McGraw Hill.
2. Computer Architecture: A Quantitative Approach: J. Hennessy and D. Patterson, Morgan Kaufmann, 3rd edition, 2003.
3. Advanced Computer Architecture and Computing: S.S. Jadhav, Technical Publication, Pune

Reference Books:

1. Advanced Computer Architectures: A Design Space Approach: DezsoSima,Terence Fountain, Peter Karsuk, Pearson Education, 1st edition, 1997.
2. Advanced Computer Architecture: Richard Y. Kausi ; Prentice Hall of India

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code : 24EE51TH0105-03 **Course : Advanced Digital Signal Processing**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Analyze the multirate digital signal processing architectures
- Describe the architecture of programmable DSP processor
- Reduce the computational complexity of the signal processing algorithms
- Illustrate the applications of DSP

Syllabus:

Basics of Signal Processing and Multirate Signal Processing

Basics of signal Processing, Multirate Signal Processing: analysis of multirate structures, multistage design of decimator and interpolator, computationally efficient interpolator and decimator structures, Design of linear phase/poly-phase FIR filters.

Programmable DSP (P-DSP) Processor : Evolution of (P-DSP) processors and features, multiport memory , Architectural structural of (P-DSP) :MAC units, Barrel Shifters , Introduction to DSP processor family for multimedia signal processing ,SIMD, MIMD, VLIW architecture,

Algorithmic strength Reduction in Filters :

Parallel FIR filters: formulation using polyphase decomposition, Fast FIR algorithms

Algorithm -Architecture Transformation : DCT -IDCT, Parallel Architecture for Rank order filters

Applications of DSP:

Dual Tone Multifrequency Signal Detection, Spectral Analysis of Sinusoidal signal and non stationary signals

Sound Processing : echo filtering , reverberator architecture, flanging, chorus generator,

Oversampling A/D and D/A convertor

Text Books

1. Digital Signal Processing : Principles, Algorithms and Applications PHI publications 4th Edition, John G. Proakis, Dimitris G. Manolakis
2. VLSI Digital Signal Processing Systems: Design and Implementation Wiley India Edition, By K.K. Parhi
3. Digital Signal Processing : A computer Based Approach , Mcgraw Hill 3rd Edition , By Sanjit K Mitra

Reference Books:

1. Discrete Time Signal Processing,Pearson Prentice Hall India , 2nd edition, A.V. Oppenheim, R.W. Schaefer

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0105-04 **Course: Hardware Assisted Security**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

After completion of the course student will be able to:

- Understand main security primitives typically used to develop defense mechanisms.
- Examine different performance parameters of hardware security primitives.
- Analyze attacks on security primitives & possible countermeasures.
- Evaluate different security applications.

Syllabus

Primer on Cryptographic Primitives & Security Attacks: known security attacks on electronics systems, main cryptographic primitives typically used to develop defense mechanisms, motivation behind the development of hardware-based security solutions, physically un-clonable functions(PUF).

PUFs Design Principles & Evaluation Metrics: the concept of physical disorder, PUF device using integrated circuit design techniques, the important metrics employed to assess the quality and usability of PUF circuit architectures.

Reliability Challenges of Silicon-based PUFs: The physical mechanisms of CMOS aging, typical temporal failure mechanisms, including radiation hits, electromagnetic interference, thermal noise, case study, Reliability Enhancement Techniques for PUFs.

Security Attacks on PUFs & possible Countermeasures: The design qualities one should consider when evaluating the security of a PUF design, adversary classification, principles of machine learning algorithms and how these can be employed to realize mathematical cloning attacks, side channel attacks.

Hardware-based Security Applications: Key generation, Authentication, Anti-counterfeiting Techniques.

Reference Books:

1. ChristofPaar, JanPelzl, “Understanding Cryptography”, 2nd edition Springer, 2010.
2. Jonathan Katz and Yehuda Lindell, “Introduction to Modern Cryptography", 3rd Edition, CRC Press, 2021.
3. Ahmad-Reza Sadeghi, David Naccache, PimTuyls, “Towards Hardware-Intrinsic Security: Foundations and Practice” Springer , 2014
4. RoelMaes, “Physically Unclonable Functions Constructions, Properties and Applications”, Springer , 2014.
5. IEEE Transactions on Information Forensics and Security.

SYLLABUS OF SEMESTER I, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0105-05 **Course: Machine Learning**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon successful completion of the course, students will be able to:

- Understand the fundamental concepts of machine learning, and get an insight of when to apply a particular machine learning approach.
- Comprehend the underlying mathematical relationship within/across Machine Learning algorithms.
- Apply machine-learning algorithms to complex engineering problems, optimize the models learned and report on the expected accuracy that can be achieved by applying the models.
- Design and implement deep neural networks for solving real-world problems in various domains and test them with benchmark data sets.

Syllabus

Foundations and paradigms of Machine Learning

Supervised learning: K-Nearest Neighbors, Decision trees, Linear and Logistic Regression – Bias/Variance Trade-off, Overfitting, Regularization, Variants of Gradient Descent, Support Vector Machines, boosting and bagging, Ensemble methods such as Random Forest and Ada Boost.

Artificial Neural Networks: Perceptron, Multilayer networks, Backpropagation algorithm, Optimization algorithms,Introduction to Deep Neural networks, Convolutional Neural Networks (CNNs) and Recurrent Neural Networks (RNNs), Brief introduction to ML applications in computer vision, and natural language processing using Tensorflow/Pytorch.

Probabilistic Machine Learning- Bayesian learning and Bayesian networks, Naive Bayes classifier; Bayes optimal classifiers, Maximum Likelihood Estimation, MAP; Gaussian Discriminant Analysis.

Unsupervised learning: Clustering, Expectation Maximization, and Gaussian Mixture Models. Dimensionality Reduction-PCA, LDA, and Feature Selection, PAC Learnability.

Text Book:

1. Understanding Machine Learning: From Theory to Algorithms, by Shai Shalev-Shwartz, Shai Ben-David, Third edition, Cambridge University Press, 2015.
2. Pattern Recognition and Machine Learning by Christopher M. Bishop, First edition, Springer, 2006.
3. The Elements of Statistical Learning Data Mining, Inference, and Prediction by Trevor Hastie, Robert Tibshirani, Jerome Friedman, Second Edition, Springer, 2009.

Reference Books:

1. Machine learning, by Mitchell Tom, First edition, McGraw Hill, 1997.
2. Deep Learning by Ian Goodfellow, YoshuaBengio, Aaron Courville, & Francis Bach, MIT Press, 2017.
3. Machine Learning: An Algorithmic Perspective by Stephen Marsland, Second Edition, Chapman and Hall/CRC, 2014
4. Richard O. Duda, Peter E. Hart, David G. Stork. Pattern classification, Wiley, New York, 2001.
5. Machine Learning: A Probabilistic Perspective by Kevin P. Murphy, Francis Bach; MIT Press, 2012.
6. Recent Research Papers from Reputed Journals and Conferences such as ICLR, NIPS, ICML, CVPR, PAMI etc.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0201 **Course: Analog IC Design**

L: 4 Hrs, P: 0 Hrs. Per week **Credits: 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Understand basics of data converters
- Apply mathematical models of MOS transistors to evaluate their behavior in analog circuits.
- Analyze MOS based analog building blocks
- Evaluate various analog IC performance parameters.
- Design CMOS analog circuits by taking suitable design approaches for given specifications

Syllabus:

Introduction to analog VLSI and analog design issues in CMOS technologies

Basic analog building blocks: Switches**,** Active resistors, current, voltage sources and sinks, current mirrors, current and voltage reference, Bandgap references.

Amplifiers, Common Source, Source follower, Common Gate and Cascode amplifiers, Frequency Response.

Frequency Response of Amplifiers: Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers

Differential Amplifier-Basic differential Pair, common mode response, CMRR, Differential Pair with MOS load, Gilbert Cell.

OPAMP Design: Single stage and two Stage OP-Amps, Frequency compensation.

Switch Capacitor circuits : General considerations, sampling switches, Switched capacitor integrator.

Data Converter Fundamentals: DAC/ADC Specifications, Data Converter Architectures: DAC architectures, Resistor String, Charge-Scaling DACs, Cyclic DAC, Pipeline DAC.ADC Architectures-Flash, The Two-Step Flash ADC, The Pipeline ADC, Integrating ADCs, The Successive Approximation ADC.

Text Books:

1. Design of Analog CMOS IC: B Razavi, Tata Mcgrw Hill (2002)
2. CMOS Circuit Design, Layout and simulation: J. Baker, D.E. Boyce., IEEE press (2010).
3. VLSI Design techniques for Analog and digital Circuits: R.L. Geiger, P.E. Allen, D. R. Holberg, OUP, (2/E) McGraw Hill (2002)

Reference Books:

I. VLSI Design techniques for Analog and digital Circuits: Randel Geiger, P Allen, N Strader, Tata Mcgraw, Hill, (2/E) (2010)

II. Analysis And Design Of Analog ICs : Paul R. Gray, Paul J. Hurst Stephen H. Lewis, Robert G. Meyer, J, Willy and Sons, (4/E) (2001)

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0201 **Course: Analog IC Design Lab.**

L : 0 Hrs., P : 2 Hrs., Per week **Credits : 1**

Practical / Case Studies/ Mini projects based on syllabus of 24EE51PR0201

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0202 **Course: System Verilog for Verification**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to

- Describe the advantages and enhancements to SystemVerilog to support verification
- Describe object-oriented programming and create a class-based verification environment
- Utilize assertions to quickly identify correct behavior in simulation
- Create and utilize random data generation and functional coverage features of system verilog for simulation verification

Syllabus:

Verification Guidelines: Introduction, Verification Process, Verification Plan, Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage, Testbench Components, Layered Testbench,

Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Creating New Types with typedef, Creating User-Defined Structures, Enumerated Types, Constants, Strings

Procedural Statements and Routines: Procedural Statements, Tasks, Functions, and Void Functions

Basic Oop: Where to Define a Class, OOP Terminology, Understanding Dynamic Objects

SystemVerilog Assertions: Types of Assertions and examples

Threads and Inter-process Communication: Working with Threads, Inter-process Communication, Events, Semaphores, Mailboxes, Building a Testbench with Threads and IPC

Functional Coverage: Coverage Types, Functional Coverage Strategies, Simple Functional Coverage Example, Coverage Options, Parameterized Cover Groups, Analyzing Coverage Data, Measuring Coverage Statistics during Simulation

Introduction to Perl – Learning perl, how can it be used for automation

Text books:

1. SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear, Springer 2006
2. Writing Testbenches Using SystemVerilog, Janick Bergeron, Springer, 2006
3. SystemVerilog for Design: A Guide to Using SystemVerilog for Hardware Design and Modeling, 2nd Edition, Stuart Sutherland, Simon Davidman and Peter Flake, Springer

Reference books:

1. Writing Testbenches: Functional Verification of HDL Models, Second edition, Janick Bergeron, Kluwer Academic Publishers, 2003.
2. Open Verification Methodology Cookbook, Mark Glasser, Springer, 2009
3. Principles of Functional Verification, Andreas S. Meyer, Elsevier Science, 2004
4. Assertion-Based Design, 2nd Edition, Harry D. Foster, Adam C. Krolnik, David J. Lacey, Kluwer Academic Publishers, 2004.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code : 24EE51PR0202	**Course : System Verilog for Verification Lab**
L : 0 Hrs., P : 2 Hrs., Per week	**Credits : 1**

Practical / Case Studies/ Mini projects based on syllabus of 24EE51PR0202

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-01/ 24EE51TH0204-01

Course: VLSI Signal Processing L : 4 Hrs., P : 0 Hrs., Per week Credits: 4

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Apply the concepts of pipelining, parallel processing, retiming, folding and unfolding to optimize digital signal processing architectures.
- Analyze data flow in systolic architectures.
- Minimize the computational complexity using fast convolution algorithms.

Syllabus:

Introduction to Digital Signal Processing Systems: Introduction, Typical DSP Algorithms, Representations of DSP Algorithms.

Iteration Bound: Introduction, Data Flow Graph Representations, Loop Bound and Iteration Bound, Algorithms for Computing Iteration Bound, Iteration Bound of Multirate Data Flow Graphs.

Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing. Pipelining and Parallel Processing for Low Power.

Retiming: Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques.

Unfolding: Introduction, An algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfoldingand Retiming, Applications of Unfolding.

Folding: Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding of Multirate Systems.

Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR systolic Arrays, Selection of scheduling vector, Matrix-Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations containing Delays.

Fast Convolution: Introduction, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.

Text Books :

1. VLSI Digital Signal Processing Systems: Keshab K. Parhi. Wiley-Inter Sciences. (1999).
2. Analog VLSI signal and information processing: Mohammed Ismail, Terri, Fiez, McGraw Hill. (1994).
3. VLSI Digital signal processing system Design and implementation: Keshab. Parthi, Wiley-Inter science, (1999).

Reference Books:

1. VLSI and Modern signal processing: kung. S. Y., H. J. While house T. Kailath, prentice hall, (1985).
2. Design of Analog - Digital VLSI circuits for telecommunications and signal processing: Jose E. France, YannisTsividls, Prentice Hall, (1994).

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-02/ 24EE51TH0204-02 **Course: RF Circuit Design**

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Understand the architectures, operation and performance specifications/ tradeoff of a RF receiver and its building blocks.
- Design and analyze impedance transformation networks using passive elements with smith charts and hand calculation.
- Understand and evaluate various performance specifications for individual blocks of receiver like filters, LNA, Mixer, Power Amplifiers by hand calculations.
- Understand the sources of nonlinearity, noise, process technology and its impact on the performance parameters of individual blocks of receiver and on receiver performance.
- Demonstrate the tools and techniques to evaluate the performance specifications of RF building blocks.

Syllabus:

Characteristics of passive components for RF circuits. Passive RLC networks. Transmission lines. Two-port network modeling. S-parameter model. The Smith Chart and its applications.

Active devices for RF circuits: SiGe MOSFET, GaAs pHEMT, HBT and MESFET. PIN diode. Device parameters and their impact on circuit performance.

Review of analog filter design: Low-pass, high-pass, band-pass and band-reject filters. RF Amplifier design, single and multi-stage amplifiers.

Low Noise Amplifier design: noise types and their characterization, LNA topologies, power match vs noise match. Linearity and large-signal performance.

RF Power amplifiers: General properties. Class A, B, AB, C, D, E and F amplifiers. Modulation of power amplifiers.

Analog communication circuits: Mixers, phase-locked loops, oscillators, Transreceiver Architecture and performance specification.

Text Books:

1. The Design of CMOS Radio Frequency Integrated Circuits: Thomas H. Lee- Cambridge University Press.

Reference Books:

1. RF Microelectronics: BehzadRazavi- McGraw Hill.
2. Design of Analog CMOS integrated circuits: BehzadRazavi- McGraw Hill.
3. RF Circuit Design: Theory & Applications: Reinhold Ludwig,GeneBogdanov

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-03/ 24EE51TH0204-03

Course: Memory Technologies L : 4 Hrs., P : 0 Hrs., Per week Credits : 4

Course Outcomes:

At the end of the course, students will be able to:

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and their testing procedures.
- Knowhow of the state-of-the-art memory chip design

Syllabus:

Random Access Memory Technologies: Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.

DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs, SRAM and DRAM Memory controllers.

Non-Volatile Memories: Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.

Semiconductor Memory Reliability and Radiation Effects: General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.

Advanced Memory Technologies and High-density Memory Packing Technologies: Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.

Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging

Text Book:

1.Ashok K Sharma," Semiconductor Memories: Technology, Testing and Reliability, PHI 1997
2.Kiyoo Itoh, "VLSI memory chip design", Springer International Edition

Reference Book:

1. Luecke Mize Care, "Semiconductor Memory design & application", Mc-Graw Hill.
2.Belty Prince, " Semiconductor Memory Design Handbook".
Ashok K Sharma, "Advanced Semiconductor Memories: Architectures, Designs and Applications", Wiley Interscience

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-04/ 24EE51TH0204-04

Course: Flexible Electronics and Sensors

L : 4 Hrs., P : 0 Hrs., Per week **Credits : 4**

Course Outcome

The course will provide an insight of the technology and applications for printed and flexible electronics.

- Acquire and develop basic concepts and understanding of thin-film electronic materials and device processing.
- Develop an understanding of emerging materials, processes, device performance, and target applications for electronics , tools for flexible electronic systems
- Understand the basic concepts for integration of thin-film devices on flexible platforms

Syllabus:

Module-1 Introduction to Flexible Electronics: Background and history, trends, emerging technologies, general applications, Introduction to Semiconductors & Circuit Elements: doping, band structure, thin- film electronic devices

Module-2: Materials for Flexible Electronics: Nanowire and nanoparticle synthesis, metal oxides, amorphous thin films, polymeric semiconductors, structure and property relationships, paper-based electronics, textile substrates, barrier materials,

Module-3: Thin-film Deposition: Processing Methods for Flexible Devices, CVD, PECVD, PVD, etching, photolithography, low-temperature process integration

Module-4: Solution-based Processes: Ink-jet printing, imprint lithography, spray pyrolysis, gravure, screen printing, multilayer patterning, and film characterization techniques, design rule considerations

Module-5 Contacts and Interfaces: Schottky contacts, Ohmic contact, relevant defects, carrier recombination, conducting polymers, Carbon-based electronics, effect of applied mechanical strain

Module 6: Applications of Flexible devices and sensors:

Thin Film Transistors: device structure and performance, electrical characterization methods for rigid and flexible devices, Displays, Organic sensors and arrays, memory devices, MEMS devices, lab-on-a-chip devices, photovoltaic, wearable sensors, Body/textile antennas, Energy Harvesting devices

Text Books:

1. William S. Wong, Alberto Salleo, Flexible Electronics: Materials and Applications, 2011, 1st Edition, Springer, New York.

2. SubhasMukhopadhyay ,Anindya Nag , Printed and Flexible Sensor Technology: Fabrication and applications, , 2021 edition, IOP Series in Sensors and Sensor Systems

Reference Books:

1. Edward Sazonov, Michael R. Newman, "Wearable Sensors: Fundamentals, Implementation and Applications", 2014, 1st Edition, Academic Press, Cambridge.

2. Kate Hartman, "Make: Wearable Electronics: Design, prototype, and wear your own interactive garments", 2014, 1st Edition, Marker Media, Netherlands.

Web Sources:

1. https://www.standardsuniversity.org/e-magazine/june-2017/fabrication-and-implementation-of-wearable-flexible-sensors/

2. https://www.nature.com/articles/micronano201643

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-05/ 24EE51TH0204-05

Course: Embedded Machine Learning L : 4 Hrs., P : 0 Hrs., Per week Credits : 4

Course Outcomes:

Upon successful completion of the course, students will be able to:

- Understand the key design considerations for embedded Machine Learning
- Understand tradeoffs between various hardware architectures and platforms
- Apply the techniques for designing of efficient hardware for machine learning algorithms
- Develop the DNN using hardware/software framework
- Analyze the architecture of DNN accelerators with given target area-power-performance metrics
- Summarise the principles of Problem solving, quantitative and/or qualitative decision making in complex situations

Syllabus:

Introduction to Machine Learning, Background and overview on Deep Neural Networks, Training versus Inference ,Applications of DNNs, Embedded versus Cloud, Key Metrics: Accuracy, Throughput and Latency, Energy Efficiency and Power Consumption, Hardware Cost, Flexibility, Scalability, Interplay Between Different Metrics.

Kernel Computation, DNN Accelerators, Operation mapping on specialized hardware

Co-Design of DNN Hardware and Algorithms: Precision reduction, Quantization , Sparsity, Activation and Weight, Compression and sparse dataflow

Computing platform: Processors- GPU, CPU, NPU
Embedded AI devices: PYNQ-Z2, Arduino UNO R3, Intel Movidius NCS2, Raspberry Pi 4, Google Coral USB Accelerator, NVIDIA Jetson Nano

Software Framework: Pytorch, TinyML, Keras, Tensorflow

Accelerator: Approximate Computing, FPGA-based Accelerators, Sparsity, Reduction precision, Systolic Arrays, HW-SW Co-Design

Case Study: Real world machine learning application and implementation.

Designing of efficient DNN models for Resource constraint applications

Text Book:

1. Efficient Processing of Deep Neural Networks, Vivienne Sze, Yu-Hsin Chen, Tien-Ju Yang, and Joel S. Emer, Morgan &cLaypool publishers (2020)
2. Practical Deep Learning for Cloud, Mobile and Edge: Real-World AI & Computer-Vision Projects Using Python, Keras&Tensorflow by AnirudhKoul, Siddha Ganju, MehereKasam, O′Reilly; Illustrated edition (2019)

Reference Book:

1. IoT and Edge Computing for Architects: Implementing edge and IoT systems from sensors to clouds with communication systems, analytics, and security, 2nd Edition, by Perry Lea, Packt Publishing Limited; 2nd Revised edition
2. Hardware Architectures for Deep Learning, by MasoudDaneshtalab , Mehdi Modarressi, Institution of Engineering and Technology
3. Recent Research Papers from Reputed Journals and Conferences such as CVPR, ICLR, NIPS, ICML, PAMI etc.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-06/ 24EE51TH0204-06

Course :VLSI Physical Design L : 4 Hrs., P : 0 Hrs., Per week Credits : 4

Course Outcome

Upon successful completion of the course, students will be able to:

I. Describe the VLSI design flow and various VLSI design styles in detail
II. Use algorithmic graph theory and combinatorial optimization techniques, as per requirement, to correctly ormulate and solve VLSI design problems
III. Explain the algorithms for partitioning, floor planning, placement and routing of VLSI circuits and use them to solve simple VLSI design problems.
IV. Describe the process of Static Timing Analysis of VLSI circuits.

Introduction to VLSI CAD: VLSI design methodologies, use of VLSI CAD tools, Algorithmic Graph Theory and computational Complexity.

High-level Synthesis: Hardware Models for High-level Synthesis, Internal Representation of the Input Algorithm, and Understanding RTL to Gate Level design mapping. Basic concept of Static Timing Analysis (STA).

Partitioning: Introduction, Types of Partitioning, Classification of partitioning Algorithm, KL algorithm.

Floor-planning: Introduction, Sliced and non-sliced planning, Polish expression, Power planning, IO Planning

Placement: Introduction, classification of placement algorithms, partition based placement, timing / congestion aware Placement

Clock Tree Synthesis: Different topologies of Clock Tree Structure. Overview on Clock Mesh implementation for High Performance designs.

Routing: Fundamental Concepts of Steiner trees, Two phases of Routing: Global routing & detailed routing, Routing Algorithms

Low Power Physical Design: Understanding Various Power Optimization algorithms (dynamic and Leakage). Overview on implementation and complexities involved in low power PD.

SOC Physical Design: Re-convergent model of VLSI SOC Design, SOC Physical design, advanced physical design of SOCs.

Text books:

1. VLSI Physical Design Automation: Theory and Practice: Sadiq M. Sait, Habib Youssef, McGraw-Hill 2004
2. VLSI Physical Design: From Graph Partitioning to Timing Closure: Jin Hu, Jens Lienig, Igor L. Markov, Andrew B. Kahng, Springer, Dordrecht2011
3. Handbook of Algorithms for Physical Design Automation: Charles J Alpert, Dinesh P Mehta, Sachin S Sapatnekar, CRC Press, 2008.
4. A Practical Approach to VLSI System on Chip (SoC) Design, VeenaChakravarthi, Springer International Publishing 2020

Reference books:

1. Physical Design Essentials: An ASIC Design Implementation Perspective: KhosrowGolshan, Springer, (2007)
2. Static Timing Analysis for Nanometer Designs: A Practical Approach: J. Bhasker and Rakesh Chadha, Springer, (2009).
3. Practical Problems in VLSI Physical Design Automation, Sung Kyu Lim, Springer, (2008), ISBN 978-1402066269
4. Algorithms for VLSI Design Automation: Sabih H. Gerez and John Wiley,(1998).
5. An Introduction to VLSI Physical Design: Majid Sarrafzadeh and C. K. Wong, McGraw Hill, (1996).
6. Algorithms for VLSI Physical Design Automation: Naveed Sherwani, Kluwer Academic Pub., (1999).

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51TH0203-07/ 24EE51TH0204-07

Course: Industry Elective L : 4 Hrs., P : 0 Hrs., Per week Credits : 4

The course will be offered by an Industry expert on latest trends in Industry.

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0205 **Course: Lab Practice - II**

L : 0 Hrs., P : 4 Hrs., Per week **Credits : 2**

Course Outcomes:

Upon the completion of this course, students will demonstrate the ability to:

- Apply fundamental principles to solve problems
- Design and execute an experimental procedure, work independently, interpret experimental results
- Draw a reasonable, accurate conclusion using suitable tools and technique

Practical / Case Studies / Mini projects

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Open Elective

Course Code: 24EEOEC51TH0207 **Course: Digital System Design with FPGA**

L : 3 Hrs., P : 0 Hrs., Per week **Credits : 3**

Course Outcomes

Upon the completion of this course, students will demonstrate the ability to :

I. Design and analyze combinational, sequential and arithmetic circuits

II. Understand digital system design flow, timing, synthesis and FPGA implementation issues.

III. solve engineering problems in the area of digital system design.

Syllabus:

Basic Digital Systems: Combinational Circuits, Sequential Circuits, Timing.

Digital System Design : Top down Approach to Design, Case study, Data Path, Control Path, Controller behavior and Design, Case study Mealy & Moore Machines, Timing of sequential circuits, Pipelining, Resource sharing.

Hardware Description language : Introduction, Behavioral, Data flow, Structural Models, Simulation Cycles, Process, Concurrent Statements, Sequential Statements, Loops, Sequential Circuits, FSM Coding, Library, Packages, Functions, Procedures, Test bench.

FSM Design: Controller (FSM), metastability, synchronization, FSM issues, timing issues, pipelining, resource sharing, case study.

FPGA : FPGA Architecture Xilinx and Altera, Logic block and routing architecture.

Text Books

1. A VHDL Primer, Third Edition : J. Bhasker, Prentice Hall, (1999).

2. Digital Systems Design Using VHDL, Second edition. Lizy Kurian John, Charles H. Roth, Cengage ; (2012)

3. Fundamental of Digital Logic with VHDL Design, Third Edition, Stephen Brown, Zvonko Vranesic, McGraw Hill Education (2012)

Reference Books

1. An Engineering Approach to Digital Design : W. Fletcher, Prentice Hall

2. VHDL for Engineers, Kenneth L. Short, Pearson Education (2009)

SYLLABUS OF SEMESTER II, M. Tech. (VLSI DESIGN)

Course Code: 24EE51PR0206 **Course: Seminar**

L : 0 Hrs., P : 4 Hrs., Per week **Total Credits : 2**

Course Outcomes:

Upon completion of this course, students should demonstrate the ability to

- Identify the contemporary topic pertaining to VLSI Design.
- Present the topics with good written and oral communication skill